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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PRADEEP SINDHU and DENNIS C. FERGUSON

Appeal 2008-0572
Application 10/004,536
Technology Center 2100

Decided: May 21, 2008

Before JAMES D. THOMAS, JAY P. LUCAS,
and THU A. DANG, *Administrative Patent Judges*.

DANG, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF CASE

Appellants appeal the Examiner's final rejection of claims 1-9, 11-20, 22-26, 28-32, 34, and 35 under 35 U.S.C. § 134 (2002). We have jurisdiction under 35 U.S.C. § 6(b)(2002).

A. INVENTION

According to Appellants, the invention is a network router that makes use of embedded memory and external memory to handle packet buffering requirements for inbound and outbound packets. In particular, the router incorporates an embedded memory device to buffer first packets. This embedded memory device is used instead of a conventional external memory device, making pins that would otherwise be used to communicate with such an external memory device available for other purposes, such as for communicating with an external memory device that buffers second data packets. As a result, using additional pins allows the router to communicate with the external memory device with increased bandwidth, thereby improving the bandwidth of the router (Spec., Abstract).

B. ILLUSTRATIVE CLAIM

Claim 1 is exemplary and is reproduced below:

1. A routing component of a router comprising:
 - a first interface to communicate data with a network;
 - a second interface to communicate data to a second routing component using a switch internal to the router, wherein the first interface and the second interface are integrated within a single integrated circuit;
 - an embedded memory within the integrated circuit;
 - a memory interface to couple the integrated circuit to an external memory; and

at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data;

wherein the control unit buffers the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

C. REJECTIONS

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Ahmadi ¹	US 5,008,878	Apr. 16, 1991
Muller	US 6,246,680 B1	Jun. 12, 2001
Mathur	US 6,424,658 B1	Jul. 23, 2002
		(filed Feb. 17, 1999)
Bass	US 6,460,120 B1	Oct. 1, 2002
		(filed Aug. 27, 1999)

Claims 1-9, 11-20, 22-26, 28-32, 34, and 35 stand rejected under 35 U.S.C. § 103(a) over the teachings of Mathur and Muller; and

Claims 1-9, 11-20, 22-26, 28-32, 34, and 35 stand rejected under 35 U.S.C. § 102(e) over the teachings of Bass.

¹ Though this reference is listed by the Examiner in the Answer as Evidence Relied Upon, none of the claims on appeal is rejected over this reference. Accordingly, we have not considered this reference in this appeal.

We affirm.

II. ISSUES

The issues are whether Appellants have shown that the Examiner erred in finding that:

- A. Claims 1-9, 11-20, 22-26, 28-32, 34, and 35 are unpatentable under 35 U.S.C. § 103(a) over the teachings of Mathur and Muller; and
- B. Claims 1-9, 11-20, 22-26, 28-32, 34, and 35 are unpatentable under 35 U.S.C. § 102(e) over the teachings of Bass.

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Mathur

1. Mathur discloses a store-and-forward network switch with an embedded memory (DRAM) and an internal token bus for control. Network switch chip 18 is a store-and-forward switch that receives packets from one of four ports A, B, C, D, stores the packets in embedded DRAM packet memory 20, and transmits the stored packets out to one or more of the four ports A, B, C, D. (Col. 5, l. 63 to col. 6, l. 2; fig. 2).
2. In alternative embodiments, FIFO buffers or pipeline latches can be inserted into the circuitry at many points, such as to and from the

embedded memory. Multiple tables or banks of embedded DRAM with different contents can be used to store packets. (Col. 13, ll. 30-34).

Muller

3. Muller discloses an input packet processing which includes: receiving and verifying incoming packets, requesting buffer pointers from shared memory manager 220 for storage of incoming packets, requesting forwarding decisions from switch fabric block 210, transferring the incoming packet data to shared memory manager 220 for temporary storage in external shared memory 230, and upon receipt of a forwarding decision, forwarding the buffer pointers to output ports indicated by the forwarding decision. (Col. 4, ll. 45-55; fig. 2).
4. The memory management is designed to achieve efficient allocation of per port buffering that is proportional to the amount of traffic through a given port. Shared memory manager 220 provides an efficient centralized interface to shared memory 230 for buffering of incoming packets. Shared memory 230 is a pool of buffers that are used for temporary storage of packet data en route from an inbound interface. The shared memory serves as an elasticity buffer for adapting between the incoming and outgoing bandwidth requirements. (Col. 7, ll. 37-57).

Bass

5. Bass discloses a network switch apparatus in which data flow handling and flexibility is enhanced by the cooperation of a plurality of memory elements and a plurality of interface processors formed on a semiconductor substrate. (Abstract).
6. In Bass, an interface device chip includes a plurality of internal S-RAMs 15 and 19, Traffic Management Scheduler 40, and Embedded Processor Complex (EPC) 12. An interface device 38 is coupled. The type of interface is dictated in part by the network media to which the chip is connected. A plurality of external D-RAMs and S-RAMs are available for use by the chip. (Col. 6, l. 59 to col. 7, l. 2; fig. 1).
7. Frames received from an Ethernet MAC are placed in internal Data Store buffers by the EDS-UP. (Col. 7, ll. 24-29; fig. 1). Frames received from the switch fabric are placed in Egress Data Store (Egress DS) buffers by an Egress EDS (34) and enqueued to the EPC. (Col. 8, ll. 46-48).
8. Embedded Processing Complex (EPC) provides and controls the programmability of the interface device chip, and includes Embedded Processors (GxH), Tree-Search Memory (TSM) Arbiter, and Instruction memory for forwarding frames. (Col. 20, l. 63 to col. 21, l. 21; fig. 12A). Interface device memory complex provides storage facilities for the EPC. The memory complex includes the Tree-Search Memory (TSM) Arbiter and a plurality of on-chip and off-chip

memories. (Col. 24, ll. 24-28). The TSM arbiter provides the communication link between the Embedded Processors (GxH) and the memories, which include 5 on-chip SRAMs, 1 off-chip SRAM, and 7 off-chip DRAMs. (Col. 24, ll. 36-41; fig. 13).

IV. PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

The legal question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) secondary considerations, if any. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966).

"The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art." *See In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991), (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)), and *In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006).

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

V. ANALYSIS

35 U.S.C. § 103(a)

Appellants argue “Mathur in view of Muller fails to teach or suggest a routing component in which data (e.g. packets) received on the same interface may be buffered differently, i.e. using either internal or external memory, based on the particular destination of the packet,” but instead “Mathur specifically teaches the use of an embedded memory for buffering all data” and that “[s]imilarly, Muller teaches use of a shared memory for buffering all data” (App. Br. 18).

Mathur discloses receiving packets from ports A, B, C, D, and storing the packets in embedded DRAM packet memory 20 (FF 1-2). Muller discloses receiving and verifying incoming packets, and transferring the incoming packet data to shared memory manager 220 for temporary storage in external shared memory 230 (FF 3-4). We agree with Appellants that, even if combined, Mathur and Muller do not disclose or suggest a control unit or a routing component which buffers data using an embedded memory internal to the integrated circuit when the destination requires forwarding the data to a second routing component of the router and/or using a switch, and

which buffers the data in an external memory when the destination requires forwarding the data to the network via a first interface, as recited in independent claims 1, 9, 18, 24, and 35, or the method comprising the forwarding steps thereof, as recited in independent claim 30.

We conclude that Appellants have shown that the Examiner erred in rejecting independent claims 1, 9, 18, 24, 30, and 35, and claims 2-8, 11-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, and 34 depending therefrom under 35 U.S.C. § 103(a). Because Appellants have shown error with respect to the Examiner's positions, we reverse the rejection of claims 1-9, 11-20, 22-26, 28-32, 34, and 35 under 35 U.S.C. § 103(a).

35 U.S.C. § 102(e)

Appellants argue that Bass does not disclose the limitations of claim 1 because “[i]n Bass, all ingress frames received from the Ethernet interface are buffered using internal memory without regard to destination, and all egress frames received from the switch fabric are buffered using external memory without regard to destination” (Reply Br. 15). In the Supplemental Reply Brief, Appellants additionally argue that “[t]he prior art clearly fails to describe a routing component including a control unit having the features recited in claim 1 for actively buffering the data differently in such situations” (Supp. Reply Br. 7).

However, Appellants' claims do not include any limitation of “actively buffering the data differently in such situations.” Appellants'

claims simply do not place any limitation on what the “control unit” is to be, to represent, or to mean, other than that the control unit buffers the data using the embedded memory and the external memory. That is, Appellants appear to be arguing that the control unit buffers the data using the internal or external memory *only* when a particular destination requires forwarding the data, and thus, Appellants’ arguments are not commensurate with the invention that is claimed.

Bass discloses enhancing data flow handling and flexibility by the cooperation of a plurality of memory elements and a plurality of interface processors, wherein Bass includes an Embedded Processing Complex (EPC) which provides and controls the programmability of the interface device chip, and includes an Instruction memory for forwarding frames (FF 5-8). As admitted by Appellants, in Bass, all ingress frames received from the Ethernet interface are buffered using internal memory, and all egress frames received from the switch fabric are buffered using external memory (Reply Br. 15). Thus, in Bass, the EPC determines the destination to forward the data frames, buffers the ingress frames using the internal memory and forwards the data frames to the destination, *including* when the destination requires forwarding the data using a switch. Similarly, the EPC buffers the egress frames using the external memory and forwards the data frames to the destination, *including* when the destination requires forwarding the data to the network. We find that Bass discloses a control unit which buffers data using an embedded memory internal to the integrated circuit when the

destination requires forwarding the data to a second routing component of the router using a switch, and which buffers the data in an external memory when the destination requires forwarding the data to the network via a first interface.

As to the other claimed elements of claim 1, Appellants provide no argument to dispute that the Examiner has correctly shown where all these claimed elements appear in the prior art. Accordingly, we find that the Appellants have not shown that the Examiner erred in rejecting claim 1 as anticipated by Bass.

Appellants do not provide separate arguments for claims 2-9, 11-20, 22-26, 28-32, 34, and 35, and thus, claims 2-9, 11-20, 22-26, 28-32, 34, and 35 fall with claim 1.

For at least the above reasons, we conclude that Appellants have not shown that the Examiner erred in rejecting claims 1-9, 11-20, 22-26, 28-32, 34, and 35 under 35 U.S.C. § 102(e).

CONCLUSIONS OF LAW

(1) Appellants have shown that the Examiner erred in finding that claims 1-9, 11-20, 22-26, 28-32, 34, and 35 are unpatentable over the teachings of Mathur and Muller.

(2) Appellants have not shown that the Examiner erred in finding claims 1-9, 11-20, 22-26, 28-32, 34, and 35 are unpatentable over the teachings of Bass.

DECISION

The Examiner's rejection of claims 1-9, 11-20, 22-26, 28-32, 34, and 35 under 35 U.S.C. § 103(a) is reversed. However, the Examiner's rejection of claims 1-9, 11-20, 22-26, 28-32, 34, and 35 under 35 U.S.C. § 102(e) is affirmed. Since we have affirmed a rejection of all claims on appeal, the decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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